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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
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| 08/965,286 | 11/06/97 | GOMI T | P97.2608 |

MMC1/0725

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| EXAMINER | |
|---|---|
| NADAV,O | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |

**DATE MAILED:** 07/25/00

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. 08/965,286 | Applicant(s) Gomi et al. |
|---|---|---|
| | Examiner ORI NADAV | Group Art Unit 2811 |

☒ Responsive to communication(s) filed on *Jun 22, 1900*.

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

**Disposition of Claims**

☒ Claim(s) *1, 3, 4, 6, 17, 19, and 20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 3, 4, 6, 17, 19, and 20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

**Application Papers**

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☒ The drawing(s) filed on *Nov 6, 1997* is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

*--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---*

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a device comprising first, second and third transistors, being formed on one substrate, as recited in claim 17, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

### *Claim Objections*

2. Claim 17 is objected to because of the following informalities: "an opposite conductive type to said epitaxial layer" should read 'an opposite conductive type to that of said epitaxial layer', since a conductivity type can not be opposite a layer .

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3, 4, 6, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. (4,379,726) or Watanabe et al. (4,258,379). Kumamaru et al. teach in figure 10 a semiconductor device comprising a first vertical high speed NPN bipolar transistor 15 and a second vertical type high voltage NPN transistor 13 having a breakdown voltage which is higher than that of the first transistor, the device including an epitaxial layer 11 formed on a silicon substrate 1, 5, wherein the first NPN transistor 15 has a first embedded diffusion layer 14 formed on an upper part of the substrate and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, the second NPN transistor 13 having a second embedded diffusion layer 5a (figure 8) formed in an upper part of the substrate and having the same conductivity type as the epitaxial layer and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer and at least as high as the impurity concentration of the epitaxial layer (column 3, lines 16 and 27-28) and having a depth greater than a depth of the first embedded diffusion layer, wherein the second embedded diffusion layer is a terminal of the second NPN transistor.

Watanabe et al. teach in figure 8 a semiconductor device comprising a first vertical high speed NPN bipolar transistor 101 and a second vertical type high voltage NPN

transistor 201 having a breakdown voltage which is higher than that of the first transistor, the device including an epitaxial layer 3 formed on a silicon substrate 1, wherein the first NPN transistor has a first embedded diffusion layer 21 formed on an upper part of the substrate and has the same conductivity type and higher impurity concentration than that of the epitaxial layer, the second NPN transistor having a second embedded diffusion layer 22" formed in an upper part of the substrate and having the same conductivity type as the epitaxial layer and having an impurity concentration less than the impurity concentration of the first embedded diffusion layer and at least as high as the impurity concentration of the epitaxial layer (figure 9) and having a depth greater than a depth of the first embedded diffusion layer, wherein the second embedded diffusion layer is a terminal of the second NPN transistor.

Although Kumamaru et al. and Watanabe et al. do not explicitly disclose a first high speed transistor and a second high voltage transistor, these features are inherent in Kumamaru et al. and Watanabe et al.s' devices, because Kumamaru et al. and Watanabe et al.s' structures are identical to the claimed structure, and the first and second embedded diffusion layers render the first and second transistors as having high speed and high voltage, respectively. Therefore, the claimed structure is considered to be in at least obvious over prior art's structures.

Furthermore, the limitations of a first transistor functioning as a high speed transistor and a second transistor functioning as a high voltage transistor is a functional

limitation. However, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 3, prior art teach a first embedded diffusion layer having a shallower depth than the second embedded diffusion layer.

Regarding claim 4, prior art teach a second embedded diffusion layer having a impurity concentration at least as high as that of the epitaxial layer.

Regarding claim 6, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a second embedded diffusion layer having an impurity concentration of 10E13 to 10E15 in Kumamaru et al. and Watanabe et al.s' devices, since it is a matter of design choice within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claims 19 and 20, prior art teach a second embedded diffusion layer and an epitaxial layer being an effective collector layers.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumamaru et al. or Watanabe et al. in view of Takemoto et al. (4,826,780). Kumamaru et al. and Watanabe et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a third vertical PNP transistor having a separating diffusion layer formed in the substrate and separating the substrate from a third embedded diffusion layer having an opposite conductivity type to the epitaxial layer. Takemoto et al. teach in figure 13 a first vertical NPN transistor, a second vertical NPN transistor and a third vertical PNP transistor formed on the substrate, wherein the third vertical PNP transistor having a separating diffusion layer 32 formed in the substrate and separating the substrate 31 from a third embedded diffusion layer 36 having an opposite conductivity type to the epitaxial layer. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a third vertical PNP transistor on the substrate in Kumamaru et al. and Watanabe et al.'s device, because it is well known in the art to form plurality of transistors of one semiconductor substrate in order to reduce the size of the device. The type of devices which are being formed depend on the requirements of the application in hand.

### *Response to Arguments*

6. Applicant argues that Kumamaru et al. do not teach a second embedded diffusion layer having an impurity concentration at least as high as the impurity concentration of the epitaxial layer. However, Kumamaru et al. teach a second embedded diffusion layer 5a having an impurity concentration N-, which is at least as high as the impurity concentration N- of the epitaxial layer 11 (column 3, lines 16 and 27-28).

### *Conclusion*

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

Ori Nadav, Ph.D.

July 24, 2000

Tom Thomas
Supervisory Patent Examiner
Technology Center 2800